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REMARKS

Claims 1-4, 10-13, and 19-28 are all of the claims presently pending in the application. Claim 10 has been amended to more particularly define the invention. Claims 21-28 have been added to more completely define the claimed invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1-4 and 10-13 were rejected under 35 U.S.C. §112, second paragraph. Claims 10-13 were rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter. Claims 1-4 and 10-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Ozawa, Japanese Patent Publication No. 08-101919, in view of Blackham, et al., U.S. Patent No. 5,619,198. Claims 1-4 and 10-13 were also rejected under 35 U.S.C. §103(a) as being unpatentable over Yoshizawa, et al., United States Patent No. 5,359,548, in view of Blackham.

These rejections are respectfully traversed.

I. THE CLAIMED INVENTION

The claimed invention (as recited, for example, in claim 1) is directed to a fixed point data generating circuit which receives a plurality of floating point data and converts the received plurality of floating point data into respective fixed point data. The fixed point data generating circuit includes a reference data determining unit for determining a reference floating point data from the received plurality of floating point data, an exponent part subtractor unit for obtaining the differences between the values of the exponent parts of the received floating point data which are not determined as the reference floating point data and a value of an exponent part of the reference floating point data, a shifting unit for shifting a mantissa part of each of the plurality of floating point data by the difference obtained for the

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corresponding floating point data, and a bit extracting unit for extracting a predetermined number of bits of each shifted mantissa part as fixed point data.

Importantly, when an overflow occurs in the bits extracted by the bit extracting unit as the fixed point data, the extracted bits are accepted as representing the maximum value (Application at page 14, lines 21-24).

In conventional circuits, it is necessary to provide a division circuit which causes a circuit scale to be large (Application at page 2, lines 11-16).

In the claimed invention, on the other hand, when an overflow occurs in the bits extracted by the bit extracting unit as the fixed point data, the extracted bits are accepted as representing the maximum value. This may help to allow the claimed invention to improve a precision of Viterbi encoding (Application at page 13, line 6 - page 15, line 5).

II. THE 35 U.S.C. §112, SECOND PARAGRAPH REJECTION

Claims 1-4 and 10-13 stand rejected under 35 U.S.C. §112, second paragraph, as allegedly indefinite. Applicant submits, however, that these claims are clear and not indefinite.

In Item 1 of DETAILED ACTION of the Office Action dated February 6, 2006, the Examiner rejected claims 1-4, 10-13, 19 and 20 under 35 U.S.C. 112, second paragraph, alleging that, from the exemplary embodiment described on line 28 of page 14 of the specification of the present application, the numerical value "0111" after saturation process is not the maximum value.

However, in the exemplary embodiment discussed on page 14 of the Application, the first bit of "0111" may be a sign bit, and other bits obtained by removing the first bit "0" from "0111" may be the maximum value "111".

As mentioned below, the specification of the present application describes an exemplary embodiment in which the first bit of "0111" is a sign bit. That is, page 11, line 13 of the present Application describes an exemplary embodiment of the claimed invention in which a mantissa part may include a sign bit. Also, page 14, lines 21-22 of the Application, states that "[h]ere,

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since there is an overflow in #2, that is, since the MSB bit (except the sign bit) is "1", ...". Therefore, in this exemplary embodiment, it is apparent that the first bit of the mantissa part may be a sign bit.

Further, on page 13, lines 12-15, the upper four bits of a mantissa part whose first bit is a sign bit may be extracted as Viterbi input data. Therefore, it can be seen that the first bit of the Viterbi input data may also be a sign bit.

From the above, in the exemplary embodiment described on page 14, line 28 of the Application, since the first bit of Viterbi input data "0111" is a sign bit, the value "0111" may become the maximum value.

Therefore, Applicant submits that the claimed invention is clearly described and explained in the Application. Therefore, contrary to the Examiner's allegations, claims 1-4, 10-13, 19 and 20 are clear and not indefinite.

In view of the foregoing, the Examiner is respectfully requested to withdraw this rejection.

III. THE 35 U.S.C. §101 REJECTION

Claims 10-13 were rejected under 35 U.S.C. §101, with the contention that they are non-statutory, in that they are directed to computer related processes that perform data computations and manipulation to produce results that are mere numbers.

Applicant notes, however, that independent claim 10 has been amended to recite "*performing Viterbi decoding with the fixed point data*".

Applicant respectfully submits that claim 10 is directed to statutory subject matter. Indeed, Applicant would point out that the method of claim 10 clearly has a practical application, such as decoding Trellis encoded signals, and so is useful. See *AT&T Corp v. Excel Communications, Inc.*, 50 U.S.P.Q.2d 1447 (Fed. Cir. 1999); *State Street Bank & Trust Co. v. Signature Financial Group, Inc.*, 149 F.3d 1368, 47 U.S.P.Q.2d 1596 (Fed. Cir. 1998).

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

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IV. THE ALLEGED PRIOR ART REFERENCES

A. Ozawa and Blackham

The Examiner alleges that Ozawa would have been combined with Blackham to form the invention of claims 1-4, 10-13, 19 and 20. Applicant submits, however, that these references would not have been combined and even if combined, the alleged combination would not teach or suggest each and every feature of the claimed invention.

Ozawa discloses a numerical converter which includes floating point registers 10a-10i, a maximum exponent detector 11, mantissa shifting devices 12a-12i and encoding devices 13a-13i and converts floating point numbers held in registers 10a-10i to integers holding a relative size by detecting the maximum exponent of the floating point numbers held in the floating point registers 10a-10i in the maximum exponent detector 11, shifting a mantissa by the differences of the maximum exponent and respective exponents in the mantissa shifting devices 12a-12i and performing encoding in the encoding device 13a-13i (Ozawa at Abstract).

Blackham discloses a number format conversion apparatus for signal processing which includes as inputs an exponent value and a mantissa value, the exponent and mantissa values representing a numerical value for a signal sample (Blackham at Abstract).

However, Applicant respectfully submits that these references are unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight. Specifically, Ozawa is intended to provide a small scale numerical converter, whereas Blackham is intended to provide hardware that supports a variety of floating point number formats (Blackham at col. 1, lines 61-63).

In fact, Applicant submits that the references provide no motivation or suggestion to urge the combination as alleged by the Examiner. Indeed, these references clearly do not teach or suggest their combination. Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

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Moreover, neither Ozawa, nor Blackham, nor any alleged combination thereof teaches or suggests *"wherein when an overflow occurs in said bits extracted by said bit extracting unit as said fixed point data, said extracted bits are accepted as representing the maximum value"*, as recited in claims 1 and similarly recited in claim 10. As noted above, this may help to allow the claimed invention to improve a precision of Viterbi encoding (Application at page 13, line 6 - page 15, line 5).

Clearly, this feature is not taught or suggested by the cited references. Indeed, the Examiner expressly concedes that Ozawa does not teach or suggest this feature (e.g., see Office Action at page 3), but alleges that Blackham teaches this feature. This is clearly incorrect.

The Examiner alleges that Blackham discloses this feature in Figure 1. Specifically, the Examiner asserts that Figure 1 discloses a "correction means (30) for correcting an overflow output from a floating-point/fixed-point conversion by representing the overflow output by a maximum value" (Office Action at page 3). However, Blackham describes the output mantissa clip circuit 30 by stating simply that it has as inputs 1) an unclipped output mantissa signal, and 2) a MAXCLIP signal, 3) the POS output signal, and 4) an overflow output from the barrel shifter 28. Blackham states that the circuit 30 clips the unclipped output mantissa signal "to a maximum level, if positive, or a minimum level, if negative, to produce an output mantissa signal in floating point number format or an output fixed point number signal in fixed point number format" (Blackham at col. 3, lines 14-26).

First, nowhere in these passages, nor anywhere else for that matter, does Blackham even teach or suggest extracting a predetermined number of bits of a shifted mantissa part as fixed point data. Thus, Blackham clearly does not teach or suggest accepting extracted bits as representing a maximum value.

Moreover, even assuming (arguendo) that Blackham would somehow be construed as disclosing accepting extracted bits as representing a maximum value, Blackham makes no mention of when or under what conditions extracted bits are accepted as representing a maximum value. Therefore, Blackham certainly does not teach or suggest that extracted bits

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are accepted as representing the maximum value when an overflow occurs in the bits extracted by the bit extracting unit as the fixed point data, as in the claimed invention.

Therefore, Applicant respectfully submits that these references would not have been combined and even if combined, the alleged combination would not teach or suggest each and every feature of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. Yoshizawa

The Examiner alleges that Yoshizawa would have been combined with Blackham to form the invention of claims 1-4, 10-13, 19 and 20. Applicant submits, however, that these references would not have been combined and even if combined, the alleged combination would not teach or suggest each and every feature of the claimed invention.

Yoshizawa discloses a floating-point arithmetic system which allows arithmetic operations to be performed for floating-point data (Yoshizawa at Abstract).

However, Applicant respectfully submits that these references are unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight. Specifically, Yoshizawa is intended to execute various arithmetic operations with small amounts of hardware at high speed (Yoshizawa at col. 7, lines 60-65; col. 8, lines 62-67), whereas as noted above, Blackham is intended to provide hardware that supports a variety of floating point number formats (Blackham at col. 1, lines 61-63).

In fact, Applicant submits that the references provide no motivation or suggestion to urge the combination as alleged by the Examiner. Indeed, these references clearly do not teach or suggest their combination. Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, neither Yoshizawa, nor Blackham, nor any alleged combination thereof

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teaches or suggests "wherein when an overflow occurs in said bits extracted by said bit extracting unit as said fixed point data, said extracted bits are accepted as representing the maximum value", as recited in claim 1 and similarly recited in claim 10. As noted above, this may help to allow the claimed invention to improve a precision of Viterbi encoding (Application at page 13, line 6 - page 15, line 5).

Clearly, this feature is not taught or suggested by the cited references. Indeed, nowhere does the Examiner even mention this feature with respect to this rejection. That is, nowhere does the Examiner assert that this feature is taught or suggested by either Yoshizawa or Blackham.

In fact, Applicant submits that the rejection based on Yoshizawa and Blackham is so general and vague that it is difficult for Applicant to fashion a response to the rejection. Indeed, nowhere does the Examiner even mention the Blackham reference with respect to this rejection, so it is impossible for Applicant to understand what features in the claimed invention the Examiner is alleging are disclosed by Blackham.

Applicant would remind the Examiner that 37 C. F. R. 1.104(b) provides that "[t]he Examiner's action will be complete as to all matters" (emphasis added), and more particularly, 37 CFR 1.104(c)(2) requires that when the Examiner rejects a claim for lack of novelty or obviousness, "the particular part relied on must be designated" by the Examiner (emphasis added). In addition, MPEP § 707.07 provides that "[w]here a claim is rejected for any reason related to the merits thereof it should be 'rejected' and the ground of rejection fully and clearly stated" (emphasis added).

In this case, the Examiner has NOT designated the particular part of the reference relied on in rejecting the claims, and has NOT fully and clearly stated any grounds for rejecting the claims. Therefore, the Office Action dated February 6, 2006, is clearly incomplete.

Further, nowhere does Yoshizawa teach or suggest this feature. Indeed, Yoshizawa merely teaches a system for executing calculations of multiple-input data by a single addition and subtraction means. The system includes a multiple input means 10, a shift amount

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determining means 11, a mantissa shifting means 12, a multiple-input adder-subtractor 13, a normalization circuit 14, a parallel comparator 20, a sequence-discrimination circuit 21, and a parallel-exponent-subtraction circuit (Yoshizawa at Figure 12; col. 11, line 55-col. 12, line 62).

However, nowhere Yoshizawa teach or suggest that his system extracts a predetermined number of bits of a shifted mantissa part as fixed point data, and clearly does not teach or suggest accepting extracted bits as representing a maximum value. Moreover, as with Blackham, Yoshizawa makes no mention of when or under what conditions extracted bits are accepted as representing a maximum value. Therefore, Yoshizawa certainly does not teach or suggest that extracted bits are accepted as representing the maximum value when an overflow occurs in the bits extracted by the bit extracting unit as the fixed point data, as in the claimed invention.

Further, as noted above, if the Examiner is alleging that Blackham discloses this feature of the claimed invention, the Examiner is clearly incorrect, as explained in detail above with respect to the Ozawa/Blackham rejection. Therefore, Blackham clearly does not make up for any deficiencies in Yoshizawa.

Therefore, Applicant respectfully submits that these references would not have been combined and even if combined, the alleged combination would not teach or suggest each and every feature of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

In summary, none of the cited references Ozawa, Blackham, and Yoshizawa (nor their alleged combination) teach or suggest the characteristic feature of the present invention mentioned above. Therefore, the present invention is not obvious and should not be rejected under 35 U.S.C. 103.

Further, with respect to the new claims 21-28, in the exemplary aspect of the claimed invention as defined by these claims, in the Viterbi decoding process, in case an overflow occurs when extracting predetermined bits from a fixed point data, a saturation processing is performed.

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None of the cited references teach or suggest the features of these newly added claims. Therefore, these newly added claims should not be rejected over Ozawa, Blackham and Yoshizawa, at least for the reasons mentioned above.

V. FORMAL MATTERS AND CONCLUSION


In view of the foregoing, Applicant submits that claims 1-4, 10-13 and 19-28, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

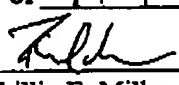
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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing Amendment was filed by facsimile with the United States Patent and Trademark Office, Examiner Ngo, Chuong D., Group Art Unit # 2193 at fax number (571) 273-8300 this 23rd day of May, 2006.


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